Design Issues in Switched Capacitor Ladder Filters

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Abstract
This paper describes the design of a switched capacitor ladder filter and explores the optimization of the Opamps for reducing power consumption. A rough but quick optimization method of the opamp is suggested depending on the settling requirement for a desired accuracy. A method for approximately analyzing the noise in different types of switched capacitor circuits is also presented. The results are compared with simulations and exhibit a close match. A prototype filter has been laid out in a .25um process and has been sent for fabrication.

1. Introduction
Switched Capacitor Filters are widely used in all signal processing and communication circuits due to their accurate parameters (governed by capacitor ratios). The basic element of these filters is a switched capacitor integrator which is used to implement a state-variable or a bi-quad active filter circuit [1]. It has been shown that passively terminated RLC ladder achieves very low sensitivity to component variations [2]. Thus a switch-cap filter based on this principle is desirable. The approach taken to designing these filters [3] is to approximate the continuous time counterparts as far as possible and minimize discrete time effects (particularly phase shifts due to time delays).

In this paper the design of a 3rd order butterworth filter in 0.25 um CMOS is presented and the various design issues, in particular the op-amp specifications for optimizing power performance are explored. Also a method for estimating the noise of different switched capacitor circuits is presented followed by simulation results which will help gain insight in the noise performance of these circuits.

2. Theory
The basic building blocks of these filters are switched capacitor integrators. Fig. 1 shows a simple integrator. The output is sampled in phase Φ1 or Φ2 and accordingly the z-transfer function is modified.

Fig.1. Simple switched capacitor integrator

\[ H_1 (z) = \frac{az^{-1/2}}{1-z^{-1}} \quad \text{and} \quad H_2 (z) = \frac{az^{-1}}{1-z^{-1}} \]  

(1)

where H1 and H2 correspond to output sampled in Φ1 or Φ2. The delay implications can be realized by substituting \( z = \exp(jwT) \). It can be shown that H2 has an additional phase term with respect to the continuous time integrators [3]. The presence of additional phase error introduces a real component which may be viewed as a lossy element. So the loops should be as delay free as possible. The magnitude error in both H1 and H2 can be reduced by increasing sampling frequency. Also minor changes in component values do not affect the performance much due to inherent insensitivity of the ladder structure [4].

2.1. Circuit Design
A 3rd order butterworth filter with a cut-off frequency, \( fc = 3.4 \text{ kHz} \) was designed. Fig 2 shows the ladder filter.

The normalized component values for a 3rd order butterworth filter are available in standard tables and are as follows: \( R_1' = 1, C_1' = 1, L_2' = 2, C_3' = 1, R_4' = 1 \).

All these values have to be de-normalized with respect to the cut-off frequency and value of termination resistance using the following transformations:

\[ C = C'/(2*\Pi*fc*Ro), L = L'*Ro/(2*\Pi*fc) \quad \text{and} \quad R = R' \quad *Ro \]  

(2)

From fig.2 the signal flow graph representation of the circuit can be obtained as in [3].

On examining the flow graph, it is evident that the integrators have to be of the form of differential integrators with two inputs.
Thus from the flow graph the transfer function of each integrator is available and so the gain ratio is known. Now the values of the capacitors and clock frequency must be chosen to avoid layout problems.

The clock frequency was taken as 100 kHz and then the values of the capacitors were calculated. The equations obtained are of the form:

$$jwRC_f = \frac{1}{jwCs_f}$$  \hspace{1cm} (3)

where $RC_f$ is obtained from the flow graph using de-normalized values of $C$ and $R$.

After calculations, the final values we arrive at are:

$$\frac{Cf_1}{Cs_1} = 4.683 \Rightarrow Cf_1 = .94 \text{ pF}, Cs_1 = 200 \text{ fF}$$
$$\frac{Cf_2}{Cs_2} = 9.36 \Rightarrow Cf_2 = 1.88 \text{ pF}, Cs_2 = 200 \text{ fF}$$
$$\frac{Cf_3}{Cs_3} = 4.683 \Rightarrow Cf_3 = .94 \text{ pF}, Cs_3 = 200 \text{ fF}$$  \hspace{1cm} (4)

Here the unit capacitance $(Cu)$ is chosen to be 200fF. A basic schematic of the final circuit is shown in fig. 3. An auto-zeroing technique has been adopted to cancel out non-ideal effects like offset and 1/f noise (discussed in detail later). The phasing of the switches is such that it minimizes delay in the loops. The switches used were NMOS switches. The sizing of the switches was determined by the minimum on-resistance needed to charge up the sampling capacitor within the clock period. Usage of CMOS switches can give an advantage as it can pass an increased range of signal voltages and also has less feedthrough due to different polarities of charge injected.

### 2.2. OTA specification

From the main circuit, the feedback factor and load capacitor for each op-amp is to be found for designing each separately.

The settling time constant, $\tau$ is the inverse of $f*GB$ where $f$ is feedback factor and $GB$ is Gain-Bandwidth. Depending on the accuracy needed, say N time constants have to be enabled within one-half clock period where this time constant is inverse of $f*GB$. So knowing the clock rate of the circuit and feedback-factor and load of the op-amps each of them can be designed according to its settling needs. This will enable saving power.

The exponential dynamic error term is $\exp(-3Ts/4\tau)$ if we consider $\tau$ of settling time $Ts$ is for slewing and remaining $3/4\tau$ is for linear settling. For N bits accuracy this is equal to $2^{-N}$. Here the design is for an accuracy of 15 bits. $Ts$ is 4.5us due to 100 kHz clock rate and an assumed non-overlap time of 0.5us. The design equation is thus

$$3Ts/4 = N*\ln(2)/(f*GB)$$  \hspace{1cm} (5)

From fig. 3, considering the integration phase the load capacitances are obtained.

For op-amp1, integration phase is $\Phi_2$. Then $Cs_2 = Cu$ acts as the load in addition to a contribution from $Cf_1$ and $Cs_1$ which is determined by the feedback factor. Basically this contribution is that of $Cs_1$ in series with $Cf_1$ which is expressible as $(1-f)*Cf_1$. Thus

$$Cload_1 = (1-f)*Cf_1 + Cu = .365\text{pF}, f = Cf_1/(Cf_1+Cu) = .82, GB >610\text{kHz}$$  \hspace{1cm} (6)

Similar calculations can be done for other opamps. Finding $C-load$ is important as it is necessary for determining phase margin and frequency response [5].

### 3. Noise Calculations

The noise spectrum for an integrator as in fig.1 has been discussed at length in [4]. Following it the spectrum at output has two parts, one continuous time component due to filtered opamp and switch noise and one due to undersampling of white noise.

The form of the sampled noise spectrum is of interest and is shown below

$$S_{sh}(w) = k\theta/\alpha C_f^2 \cdot |\sin(c/f/fs)|^2 \cdot |1/\sin(c/f/fs)|^2$$

Thus there is a huge piling up of noise at low frequencies due to undersampling of white noise which essentially submerge any flicker noise component of the opamp.
3.1. Gain and offset compensation

Some of the non-idealities that affect the performance of switched capacitor circuits are offset voltage and finite gain of the op-amp. Also the dynamic range of the circuit is affected by the aliasing of noise into base-band. One of the techniques to combat this effect is the Correlated Double Sampling method as in fig.4.

![Fig. 4. CDS compensated Integrator.](image)

The operation of the circuit makes the node x acts as a better virtual ground. Also for noise signals with low bandwidth (like the 1/f sort of noise) this method is effective as the error transmitted to the output is of the order of $N(T)-N(T-1)$ where $N(t)$ is the noise signal. This error is likely to be smaller than $N(T)$ as the noise is correlated since it has less bandwidth.

3.2. Complex Systems

Correlated Double Sampling is not always used to reduce the noise contributions as it may sometimes be inherently reduced by the topology of the systems. The methods shown will enable us to easily get the order of magnitude of the noise. This can be understood by studying the topology in fig.5 where there is an internal feedback. The corresponding difference equation is:

$$V_o(n) = V_o(n-1)+\alpha V_i(n-1/2)-\alpha V_o(n)+\alpha R_1(n)-\alpha R_2(n)$$

(Assuming $C_0 = C_s$) where $R_1(n)$ is sampled noise of resistance in upper path and $R_2(n)$ is same for switch resistance in feedback path.

![Fig. 5. Integrator with self feedback](image)

$$V_o(z) = \frac{\alpha z^{-1}}{1+\alpha - z^{-1}}V_i(z) + \frac{\alpha}{1+\alpha - z^{-1}}R_1(z) - \frac{\alpha}{1+\alpha - z^{-1}}R_2(z)$$

(8)

Let $H(w) = \frac{\alpha z^{-1}}{1+\alpha - z^{-1}}$

Here as $w \to 0$, $|H| = \alpha/\alpha = 1$. Thus it is evident that this sort of structure does not have the problem of excessive piling up of noise. This can also be seen as a type of CDS method as a part of the output is being subtracted from the input. So the correlated noise gets cancelled. To simplify the calculations of the integrated output noise power, we consider the integrated noise from the individual sources and multiply them by the proper transfer functions. This is equivalent to assuming uniform spectrum of the various noise sources. So

$$N(w) = (4kT/C_s)|H(w)|^2 + a(w)*4*Res2 + b(w)*Op(w)$$

(9)

where $Res2$ is noise spectrum due to on resistance of switch in phase $\Phi_2$, $a(w)$ is its transfer function to the output, $Op$ is op-amp noise spectrum and $b(w)$ is the transfer function this noise has to the output.
A cascade of two such integrators can be easily tackled and is not shown here. Next two integrator feedback loops as in fig.6 are considered which are inherent in switched capacitor filters.

![Two Integrator loops](image)

So this analysis is of importance to gain insight into noise analysis of general switched capacitor systems. Here let $C_0 = C_s$ and let $C_s/C_f = \alpha$.

The difference equations are:

$$V_4(n) = V_4(n-1) + \alpha^* V_3(n-1/2) - \alpha^* V_4(n) + \text{Op}_4(n) + \alpha^* R_4(n-1/2)$$  \hspace{1cm} (10)

$$V_3(n) = V_3(n-1) + \alpha^* V_2(n-1/2) - \alpha^* V_4(n-1/2) + \text{Op}_3(n) + \alpha^* R_3(n-1/2)$$  \hspace{1cm} (11)

Here $\text{Op}_j(n) =$ Noise contribution of op-amp of $j$-th stage at the output of $j$-th stage and $R_j(n) =$ Switch resistance noise of $j$-th stage. From (11)

$$(1-z^{-1})V_j(z) = \frac{\alpha z^{-1/2}}{1-z^{-1}} V_i(z) - \frac{\alpha z^{-1/2}}{1-z^{-1}} V_j(z) + \frac{\alpha z^{-1/2}}{1-z^{-1}} R_j(z) + \frac{1}{1-z^{-1}} \text{Op}_j(z)$$

From (10) and (12)

$$V_4(n) = \frac{(1-z^{-1})(1+\alpha - z^{-1})}{1+\alpha - z^{-1}} (\frac{1}{1+\alpha - z^{-1}} \text{Op}_4(z) + \frac{\alpha z^{-1/2}}{1+\alpha - z^{-1}} R_4(z)) + \frac{(1-z^{-1})(1+\alpha - z^{-1})}{1+\alpha - z^{-1}} (\frac{\alpha z^{-1/2}}{1+\alpha - z^{-1}} V_3(n) + \frac{\alpha z^{-1/2}}{1+\alpha - z^{-1}} \text{Op}_4(z))$$

Thus it is apparent that $\text{Op}_4(z)$ and $R_4(z)$ are being shaped by a zero of form $(\alpha - z^{-1})$ and so mainly noise from the first stage will contribute to total output noise.

### 4. Simulation Results

Simulation of the filter and switched capacitor blocks were done using BSIM3V3 models in 0.25 um process. The OTA was a fully differential two stage miller compensated OTA with common mode feedback. The filter was simulated in all process corners and the frequency response obtained is plotted in fig.7. The total current drawn was 230uA. Results of noise calculations are shown in Table 1.

![Frequency response of filter in typical, nfps and nsps cases compared with theoretical curve](image)

**Table 1: Comparison of theoretical and simulated results**

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### 5. Conclusion

The methods described in the paper reduce static current drained by each opamp without hampering performance thus reducing power consumption. Also the method for estimating noise in switched capacitor systems tally with simulations. A prototype of the filter has been sent for fabrication in National Semiconductor’s .25um CMOS8 process and measurements will be done on that.

### 6. References


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