Above Threshold pFET Injection Modeling intended for Programming Floating-Gate Systems

Paul Hasler* and Arindam Basu† and Scott Koziol‡
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, Georgia 30332–0250
Email: *phasler@ece.gatech.edu, †arindamb@ece.gatech.edu, ‡skoziol@ece.gatech.edu

Abstract—We present a first-order model for pFET hot-electron injection that is consistent for subthreshold and above threshold current levels. Injection is a critical phenomena for high-precision programming of floating-gate devices, and accurate modeling fuels continued improvement of programming techniques. Previous work has shown good modeling for subthreshold operation; in this work we extend the modeling throughout the region, enabling improved programming algorithms for floating-gate switch elements, resistors, and high-performance circuit elements. We discuss the implementation of this model in CADENCE’s version of SPICE.

I. IMPORTANCE OF MODELING HOT- ELECTRON INJECTION FOR ABOVE-THRESHOLD CURRENTS

Over the last decade, the number of applications of programmable floating-gate circuits has grown exponentially, powered primarily because of the ability to precisely program arrays of floating-gate devices (e.g. [1]). These advances have always followed modeling developments of the programming mechanisms for floating-gate circuits. The modeling of hot-electron injection, in particular, has led to highly effective programming for arrays of devices. The first model of hot-electron injection from first-principles physics for nFETs was in 1997, and for pFETs in 2001 / 2003 [2]. These modeling efforts focused on MOSFETs operating with subthreshold currents, where the high-field region is independent of the current gating mechanisms.

This paper focuses on developing an above-threshold hot-electron injection model for pFET devices suitable for simulation. This model is consistent for a saturated device from subthreshold to above-threshold operation. Figure 1 frames the problem and application we are considering. In particular, we are looking at programming elements configured in an array of devices Fig. 1b) since most applications in current use have anywhere from 10 to 100,000 floating-gate elements in a single IC. The theory for hot-electron injection with subthreshold currents is understood, but many applications use and program using above-threshold currents. The modeling for above-threshold currents has been based not on theory, as in the subthreshold case, but on heuristics that often fail for complex systems. Injection modeling has driven the rapid progress of floating-gate programming, and new modeling of this process opens up a range of new possibilities. Some of these examples include floating-gate switch transistors [3], floating-gate based resistor elements, high-performance analog IC elements [4], [5], tunable digital circuits, and indirect floating-gate programming [6].

In this paper, we will focus on giving the basic overview of pFET hot-electron injection modeling for subthreshold currents, extend this theory qualitatively and quantitatively towards above-threshold currents, show experimental data measured from a pFET device in an array of devices, regress the data to show the physics behavior, and compare experiment to first-order theory developed. The modeling can be directly implemented, at varying degrees of complexity, in a range
of simulation tools. We measured our experimental data from an IC we designed and fabricated in 0.35μm CMOS process available through MOSIS.

II. SUBTHRESHOLD pFET INJECTION

Figure 2 shows qualitatively hot-electron injection for a pFET device operating with subthreshold currents. Holes transport through the channel region, shown in cross section in Fig. 2a, by diffusion, as seen in the band diagram in Fig. 2b. Usually one assumes that when the holes reach the drain-to-channel depletion region, the resulting electric field transports the holes to the drain edge. Taking a closer look at the transport (inset of Fig. 2a), the holes can gain enough energy by the electric field at event (1) and impact ionize to create two holes and one electron. Electrons and holes can gain significant energy from the conduction or valance band, respectively, if the resulting localized gradient in potential is greater than the maximum strength of an optical phonon to restore the carrier to the band edge; for electrons this requires a field nearly 10V/μm, and holes are somewhat larger. The resulting electron will move back towards the channel, accelerated by the resulting fast decrease in potential (conduction-band diagram of Fig. 2b). Most of these electrons move to the resulting substrate, where they can be directly measured as current from the well terminal, as seen in event (2). Some of the electrons gain energy through the high-field region; if they gain energy greater than the Si-SiO₂ barrier (≈ 3.04eV) they can enter into the oxide region. Once in the oxide region, electrons transport by drift (event (3)) depending upon the field; for a pFET device, the band-diagram where most injection occurs will be favorable for electrons to reach the gate terminal (Fig. 2d).

These effects can be modeled from first principles, one can model the injection current (Inj) as a function of channel current (Iₛ), and drain-to-channel potential (Φdc) as

\[ I_{\text{inj}} = I_s e^{f(\Phi_{dc})} \]  

where \( f(\cdot) \) is a rational function. In practice, \( f(\cdot) \) can be approximated by a linear function over a reasonable range of injection current [7], resulting in the expression

\[ I_{\text{inj}} = I_{inj0} I_s e^{-\Delta\Phi_{dc}/V_{inj}} \]  

where \( \Delta\Phi_{dc} \) is the change in \( \Phi_{dc} \) from the bias point which created its bias injection current \( I_{inj0} \) when biased at the threshold current \( I_{th} \), and \( V_{inj} \) is a device parameter dependant upon the biasing of the drain-to-channel region. An important part of the device modeling is determining the size of \( \Phi_{dc} \).

III. ABOVE-THRESHOLD pFET INJECTION

For hot electron injection, we need to get a sufficient voltage drop in a short distance, which is defined as a local electric field above 10V/μm to generate high-energy holes. Figure 3 shows the valance band-diagram for different subthreshold and above-threshold floating-gate voltage (Vfg) biases. Subthreshold we have only the drain-to-channel region as the high-field region; therefore, only the barrier governing the channel current creates a change in the channel potential. The channel potential is proportional to \( \kappa V_{fg} \), where \( \kappa \) represents the capacitive coupling of the floating-gate voltage to the channel potential. In above threshold we need to look at the drop across the channel region as well to determine if this can improve or decrease injection (Fig.3b). In the channel region, the average electric field is the overdrive voltage over the
effective channel length \(l\). For moderate overdrive voltages (i.e., 300mV) for a minimum length 0.35\(\mu\)m transistor, the field in the channel is roughly a factor of 10 less than the critical field needed for holes to gain sufficient energy above the valence band. Therefore, the high-field region that enables hot-carrier transport is still the drain-to-channel region, which is not reduced by the resulting overdrive for this device, which is expressed as \(\kappa(V_g - V_{T0}) - V_s\) for the threshold voltage \(V_{T0}\) and well referred source \(V_s\) and gate \(V_g\) voltages. The result is that the channel potential, where the source side moves very little above threshold, again changes proportionally to \(\kappa V_g\). Therefore, we can model the subthreshold and above-threshold injection current as

\[
I_{inj} = I_{inj0} \left( \frac{I_s}{I_{th}} \right)^{\frac{-\kappa \Delta V_{fg}}{V_{inj}}} e^{-\Delta V_{ds}/V_{inj}} \tag{3}
\]

The injection current increases as subthreshold current increases, but as the current goes above threshold the injection current efficiency decreases and eventually the injection current decreases as current increases.

**IV. EXPERIMENTAL pFET INJECTION MEASUREMENTS**

This section considers the experimental measurements for a pFET transistor in an array of devices with the typical infrastructure used to program arrays of pFET devices [8], [1]. The pFET devices are injected by ramping up the power supply, applying the desired \(V_{ds}\) for a short pulse time \(T = 10\mu\)s, and then ramping the power supply back down. We measure the current when the devices are ramped down, and adjust the gate voltage when ramped up to be injecting at a similar current. By measuring the source current, we can compute the injection current \(I_{inj}\) as

\[
I_{inj} = -C_T \frac{dV_{finj}}{dt} = -C_T \frac{dV_s}{dI_s} \frac{dI_s}{dt} \approx -C_T \frac{I_s \Delta I_s}{g_m I_s} \tag{4}
\]

\(C_T\) is the total capacitance at the floating-gate node, which is approximately 10fF for our device, and \(g_m\) is the transcon-
We computed these values by using the percentage change in source current, normalized by $g_m / I_s$, and divided by $g_m / I_s$ result. Theory matches well with experimental measurements. Further, we present a first-order model for pFET hot-electron injection that is consistent for both subthreshold and above threshold current levels. We extended the subthreshold operation modeling throughout the MOSFET operating region (in saturation). These techniques should enable improved programming algorithms for floating-gate switch elements, resistors, and high-performance circuit elements. We discussed how this modeling can be directly implemented in a range of simulation tools, primarily targeted towards implementing this model in CADENCE’s version of SPICE. This implementation will be described at the conference, and not presented here because of space considerations. Further, since this data was taken in array, one could easily extend these techniques to modeling the device statistics over the entire array.

**References**